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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/616,396	07/09/2003	Matthias Goldbach	Z&P-INF-N10309	9802

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EXAMINER	
HARRISON, MONICA D	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 06/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/616,396	GOLDBACH ET AL.
	Examiner	Art Unit
	Monica D. Harrison	2813

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 7/9/03
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Rajeevakumar (6,658,816).

2. Regarding claim 1, Rajeevakumar discloses a method for fabricating trench capacitors for memory cells having at least one selection transistor for integrated semiconductor memories, which comprises the steps of: providing a semiconductor substrate of a first conductivity type (Figure 2, reference 200); producing a horizontal mask on the semiconductor substrate, the horizontal mask to be used for producing trenches (Figure 2, references 204, 206, and 208); carrying out an anisotropic etching step after a completion of the horizontal mask (column 2, lines 62-67 thru column 3, lines 1-3), thereby producing upper trench regions in the semiconductor substrate (Figure 2, reference 210); covering sidewalls of the upper trench regions with vertical masks (Figure 2, reference 212); etching the semiconductor substrate selectively with respect to the horizontal mask and the vertical masks, for producing lower trench regions (Figure 3, reference 310); doping surfaces of the lower trench regions with a material of a second

conductivity type resulting in first electrodes being produced on surfaces of the lower trench regions (Figure 6, reference 620); applying a dielectric to the first electrodes (Figure 6, reference 618); removing the vertical masks (column 3, lines 31-42); applying second electrodes to the dielectric resulting in the trench capacitors being formed in the lower trench regions (Figure 5, reference 510); etching the semiconductor substrate in the upper trench regions after an application of the second electrodes (column 3, lines 2-42); producing an insulator on a region etched in each of the upper trench regions (Figure 1, reference 622); and producing electrically conductive connections each connecting a respective one of the second electrodes to a respective selection transistor (Figure 1, reference 6; *buried strap which is connected to the gates*).

3. Regarding claim 2, Rajeevakumar discloses forming the semiconductor substrate from one of silicon and p-doped silicon (Figure 2, references 200 and 202).

4. Regarding claim 3, Rajeevakumar discloses producing the horizontal mask as a layer stack (Figure 2, references 204, 206, and 208) using a photolithographic process (column 2, lines 25-34).

5. Regarding claim 4, Rajeevakumar discloses forming the layer stack to have at least one of a nitride layer (Figure 2, reference 204) and an oxide layer (Figure 2, reference 206).

6. Regarding claim 5, Rajeevakumar discloses affecting the anisotropic etching of the semiconductor substrate using a dry etching process (column 3, lines 2-3).

7. Regarding claim 6, Rajeevakumar discloses forming the upper trench regions in each case to project into the semiconductor substrate to a depth of about 500 nm to 1500 nm (column 2, lines 59-60).

8. Regarding claim 7, Rajeevakumar discloses which further comprises producing the vertical masks by conformally depositing a covering layer and subsequent anisotropic etching the covering layer (Figure 4, reference 414).

9. Regarding claim 8, Rajeevakumar discloses forming the covering layer from at least one material selected from the group consisting of nitrides and oxides (Figure 4, reference 414; *oxide*).

10. Regarding claim 9, Rajeevakumar discloses producing the lower trench regions by anisotropic etching (column 3, lines 31-42)

11. Regarding claim 10, Rajeevakumar discloses enlarging a surface of the lower trench regions by isotropic etching (column 3, lines 31-42).

12. Regarding claim 11, Rajeevakumar discloses forming the trenches to have a depth of about 5 um to 15 um (column 2, lines 59-60).

13. Regarding claim 12, Rajeevakumar discloses enlarging a surface of the lower trench regions by producing mesopores in a manner subsequent to the etching of the lower trench regions (Figure 5, reference 510).

14. Regarding claim 13, Rajeevakumar discloses wherein the doping of the lower trench regions connects the first electrodes of adjacent trenches to one another in a low-impedance manner (Figure 1).

15. Regarding claim 14, Rajeevakumar discloses wherein the dielectric completely covers the first electrodes in the lower trench regions (Figure 6, reference 618).

16. Regarding claim 15, Rajeevakumar discloses forming the dielectric as a layer selected from the group consisting of an oxide-nitride-oxide layer, a nitride-oxide layer, an oxide

layer, an Al_2O_3 layer, a Ta_2O_5 layer, a hafnium oxide layer, a layer containing Al_2O_3 and a combination of these layers (Figure 2, references 204, 206, and 208).

17. Regarding claim 16, Rajeevakumar discloses converting the nitride-oxide layer into an oxide layer in the upper trench regions (Figure 2, references 204, 206, and 208).

18. Regarding claim 17, Rajeevakumar discloses producing the second electrodes by filling the trenches with a conductive material as far as the upper trench regions (Figure 6, reference 620).

19. Regarding claim 18, Rajeevakumar discloses using doped polysilicon as the conductive material for forming the second electrodes (Figure 6, reference 620).

20. Regarding claim 19, Rajeevakumar discloses replacing the vertical masks with the insulators having a low dielectric constant after a production of the second electrodes (Figure 6, reference 618).

21. Regarding claim 20, Rajeevakumar discloses forming the insulators from silicon oxide (Figure 6, reference 618).

22. Regarding claim 21, Rajeevakumar discloses forming the insulators with a predetermined layer thickness (Figure 6, reference 618).

23. Regarding claim 22, Rajeevakumar discloses electrically conductively connecting each of the second electrodes of the trench capacitors to a diffusion location of the respective selection transistor (Figure 1).

24. Regarding claim 23, Rajeevakumar discloses removing the horizontal mask (column 2, lines 61-63).

25. Regarding claim 24, Rajeevakumar discloses removing the vertical masks before applying the dielectric (column 3, lines 31-42).

26. Regarding claim 25, Rajeevakumar discloses removing the dielectric in the upper trench regions (Figure 4, reference 414).

27. Regarding claim 26, Rajeevakumar discloses producing the insulators on the semiconductor substrate in the upper trench regions after removing the vertical masks (Figure 6, reference 622).

28. Regarding claim 27, Rajeevakumar discloses forming a liner in the upper trench regions (Figure 6, reference 622); and etching selectively the semiconductor substrate with respect to the liner in the upper trench regions after applying the second electrodes (Figure 6, reference 620; column 3, lines 31-42).

29. Regarding claim 28, Rajeevakumar discloses during the etching in the upper trench regions, opening the semiconductor substrate with an aid of double etching-back of the second electrodes (column 3, lines 31-42).

30. Regarding claim 29, Rajeevakumar discloses performing the application of the dielectric: which further following steps after an filling the trenches with a material forming the second electrodes (Figure 6, reference 620); etching-back the material forming the second electrodes as far as a first etching-back step within the upper trench regions (column 3, lines 31-42); covering trench walls above the first a liner (Figure 6, reference 618); etching-back step with etching-back the material forming the second electrodes as far as a second etching-back step (column 3, lines 31-42); and opening the semiconductor substrate selectively with respect to the liner (Figure 6).

31. Regarding claim 30, Rajeevakumar discloses applying the liner to (Figure 6, reference 618) one of the dielectric (Figure 6, reference 622) and the semiconductor substrate (Figure 6, reference 200).

32. Regarding claim 31, Rajeevakumar discloses applying the liner to the dielectric (Figure 6, reference 618); and converting the liner into an oxide (Figure 5, reference 516).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica D. Harrison whose telephone number is 571-272-1959. The examiner can normally be reached on M-F 7:00am-3:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Monica D. Harrison
AU 2813

mdh
June 21, 2005

Craig A. Thompson

CRAIG A. THOMPSON
PRIMARY EXAMINER